#10A/12-2-03
V-Jones

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Takaki YOSHIDA et al.

Serial No.: 09/697,305

Filed: October 27, 2000

Group Art Unit: 2133

Examiner: Joseph D. Torres

For: FAULT DETECTING METHOD AND LAYOUT METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the Office Action mailed May 28, 2003, please amend the above-identified application as follows: